

Introduction: Intelligent camera system is currently a hot topic in computer vision research. The goal of intelligent video is to process the captured video from the monitored area, extract specific information and take appropriate action based on that information. Due to the high computational complexity of vision tasks and the real time nature of these systems, current software-based intelligent video surveillance systems are unable to perform sophisticated operations. Embedded processing can execute low-level tasks within the camera platform, before data transmission to the host system. Cameras with embedded processing resources are known as "Smart Cameras", and are the subject of growing interest.

PICSY Project

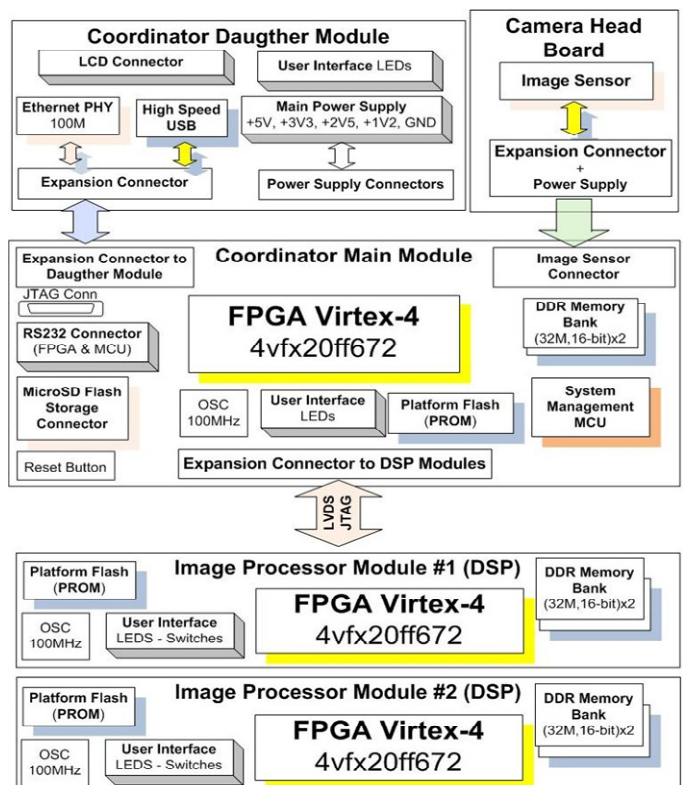
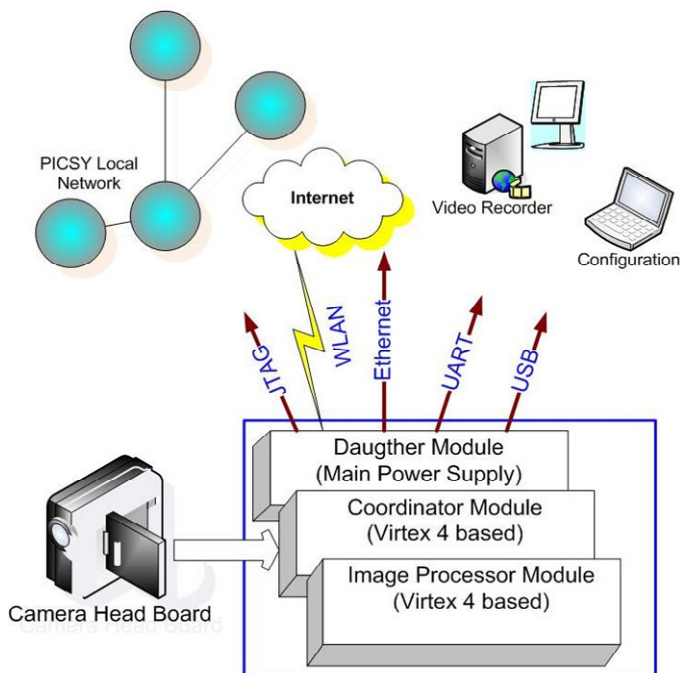
The **PICSY** project is the development of Cooperative Camera system to develop a flexible and extensible monitor to track the state of the surrounding neighborhood, which serves as the basis for a powerful and flexible approach to intelligent camera. The primary step of this project was to develop a hardware platform primarily targeted at real-time image processing. The developed system is capable of streaming image data from a camera headboard, through a Virtex-4FX20 FPGA for processing, and for analysis. It offers a host of real world interfaces including high speed USB and Ethernet connectivity. In the PCB design we have given a good consideration to high frequency design and also transmission lines. The designed PCBs are simulated based on the IBIS models and physical PCB layer stack up definitions.

To shrink the board dimension, some parts were moved off the main board to daughter board and have it to fit inside camera chassis.

Linux is used as the operating system on the Power PC 405 processor (hard core inside FPGA) as it offers a solid, familiar platform for development with a feature-rich toolchain.

Applications

- **Video surveillance systems** : are becoming increasingly important in public access facilities such as airports, transport stations and banks to provide security.
- **Distributed visual processing for a home visual sensor network** : Recently, the focus of robotics industry is moving from industrial robots to personal service robot. Personal service robots are expected to play an important role as interactive assistants for health care, entertainment, education, and home cleaning.
- **In-Vehicle Processor for Driver Assistance Systems** : Vision processing (or image recognition) is the subject of high expectations as a promising function for assisting drivers to improve driving safety.
- **Industrial Vision System** : An industrial vision system must perform a specific and unambiguous inspection. The examination result is crucial to determine if the analyzed item can keep on its transformation process into the production line.

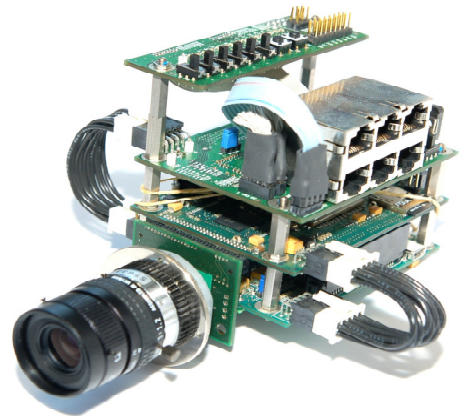
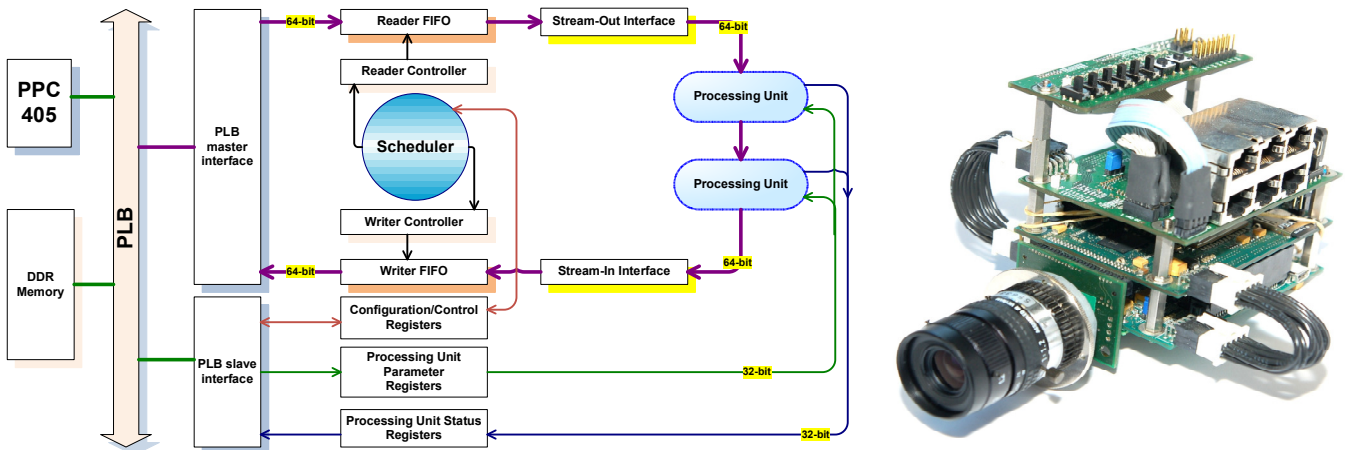


PICSY Board Stack up Modules

- **Coordinator Main Module** based on Virtex-4 FX20(FF672 Package) with one bank of DDR memory and LVDS connection to the DSP module with an interface to Image Sensor.
- **Coordinator Daughter Module** as host for High Speed USB and PHY ETH (100M) and also the Main Power Supply of system. This board has a connection with the Coordinator Module in the stack-up structure.
- **DSP Module** based on Virtex-4 FX20(FF672 Package) with two bank of DDR memories and LVDS connection to the Coordinator module.
- **Camera Head Board Module** as host for image sensor, C-Mount and Lens (Objective). This board has a connection with the Coordinator Main Module.

System on Chip design

- A system on chip (**SoC**) is usually made up of a processor connected to a set of peripherals and dedicated hardware modules via a bus system. In video streaming applications in which large amount of data must be computed in real time, this traditional system architecture is no longer viable because the bus becomes a bottleneck. The programmability and the seamless use of hardware accelerators in image processing application is insured through the design and implementation of a streaming data interface. By porting the Intel's OpenCV computer vision library to the system, software developers do not need to recompile their code in order to use the platform.
- In the **SoC** design part, the major focus is on the implementation of a concept which connects physical external memory to the several implemented application oriented processor units, to supply them by required raw stream data and to restore processed results get back to memory without intervention of main processor (Power PC). This interface has been called Streaming Data Interface (SDI) and plays major role in the whole performance of system.

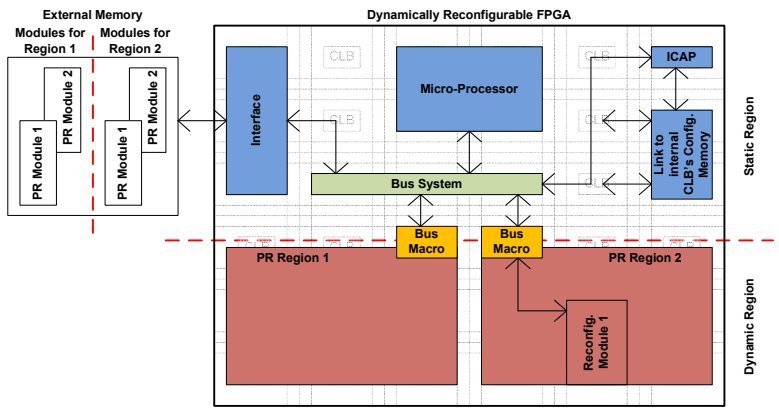


Rich Image Processing library with hardware accelerator

- By porting the Intel's OpenCV computer vision library to the system, software developers do not need to recompile their code in order to use the platform.
- Our goal is to build a complete solution for software developers to have an accelerated System on Chip to perform their OpenCV algorithms. In hardware-software-co-design the data flow analysis plays an important role because the communication between modules can heavily influence the performance of the system. Our architecture offers a wide spectrum of possibilities to interconnect modules and to let data flow.

Hardware Dynamic Partial Reconfiguration

Dynamic Partial Reconfiguration techniques are used to modify the SoC architecture at run-time. This allows the addition of new hardware modules without service interruptions. Such complex system requires to divide the SoC into a static and a dynamic regions. Dynamically reconfigurable regions are separated from the static region by fix interfaces called *bus macro*. All control and data signals must pass through them. Reconfigurable Modules are stored in an external memory in the form of a file called *bitstream*. Thanks to a Linux operating system, bitstreams files can be managed and exchanged on a network.



Typical Application: Contour and Histogram extraction by PICSY in driver assistance

