Reducing X-Masking Data Volume and Load Time
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Short Description

The invention is a highly effective x-masking architecture for large scan designs with a high percentage of unknown values. The masking logic allows defining arbitrary, pattern-specific masks for filtering unknown values and provides an efficient mechanism for the parallel loading of x-masking information via scan chains. Compared to Cadence WIDE-1 solution, the invention reduces mask data volume by 70% and mask load time by 90% – 99%.

Idea

The invention provides a memory element each to store the mask information for each scan chain. Depending on the x-distribution, only the memory elements for scan chains actually capturing unknown values are configured to form the mask register (figure 1). This dynamically created mask register is divided into *g* segments of equal length using a special intake position register. Each segment is fed by a separate scan chain (figure 2). The number of segments depends on the number of independent bit values which can be set by the decompressor. Compared to serial mask loading, load time is reduced by a factor of *g*.

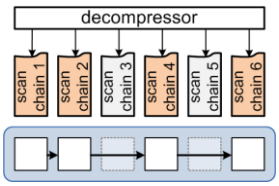


Fig. 1: forming mask register

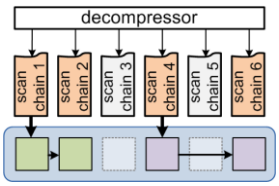
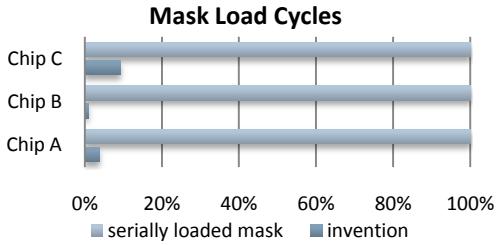


Fig. 2: loading segments

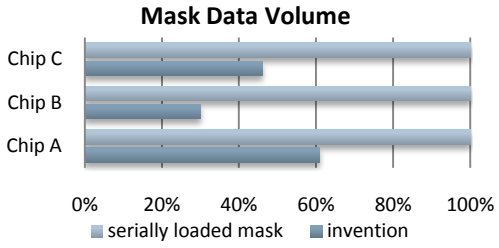
During test, only reduced pattern specific mask data is loaded for each pattern; a mask-enable signal determines the clock cycles in which x-masking is to be performed.

Results

The following diagram depicts the number of shift cycles required to load a new mask pattern. Cycle count of the invention is compared to a serially loaded mask, e.g. Cadence WIDE-1.



Using the invention, only mask data for scan chains actually affected by unknown values must be provided. This reduces mask data volume by 40%-70% compared to conventional mask registers like WIDE-1.



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