Software-Managed Cache Coherence for fast One-Sided Communication

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Motivation

- Will future many-core systems provide hardware cache coherence?

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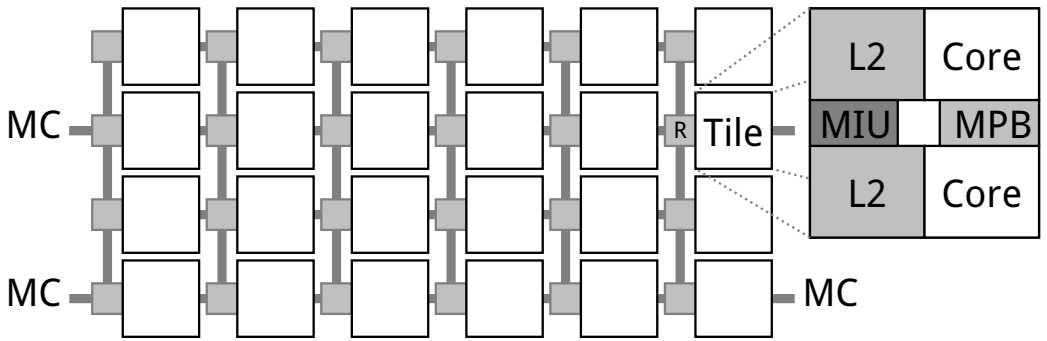

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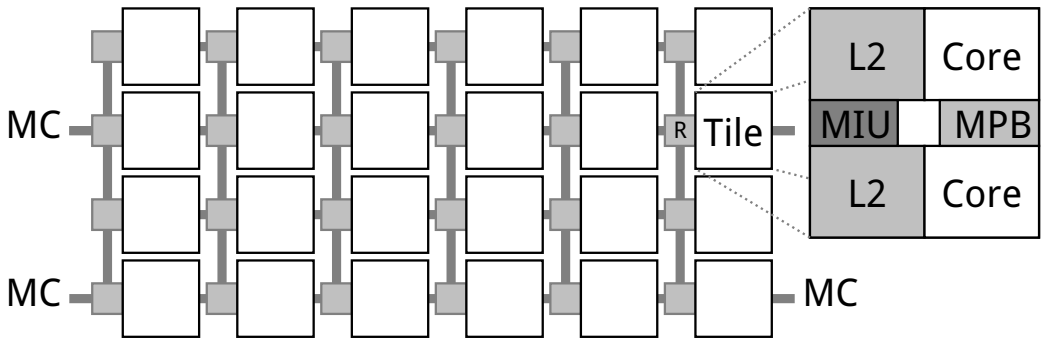

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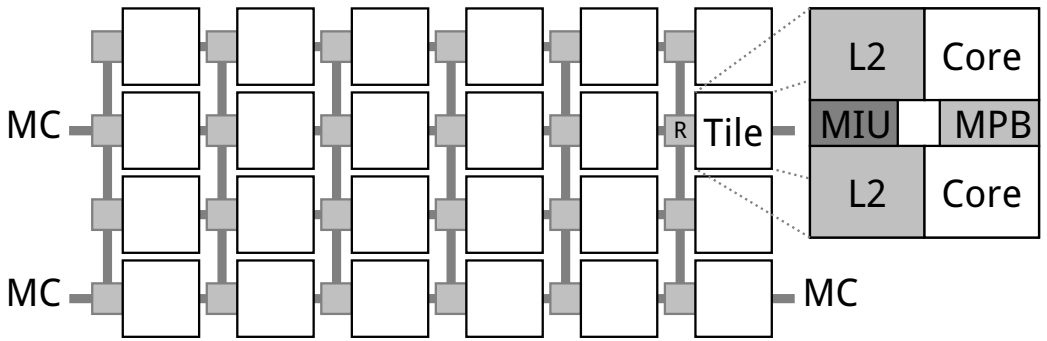

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- new approach: use shared memory on nCC CPU for **one-sided communication** and **manage cache coherence in software**

MPI One-Sided Communication

origin **target**

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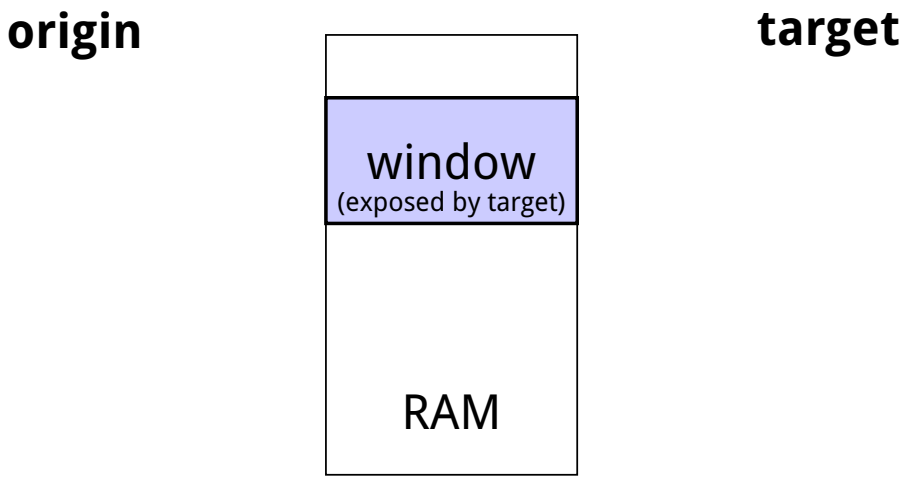

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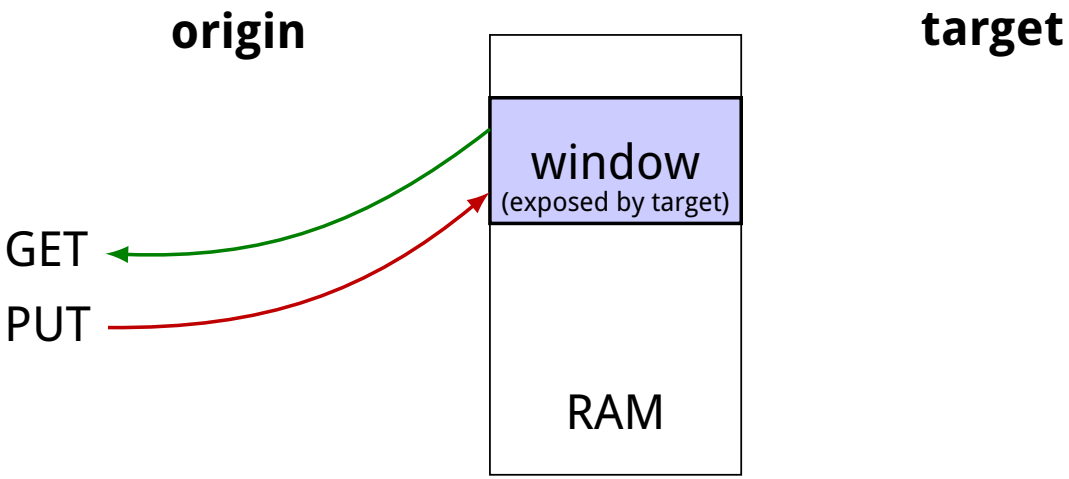

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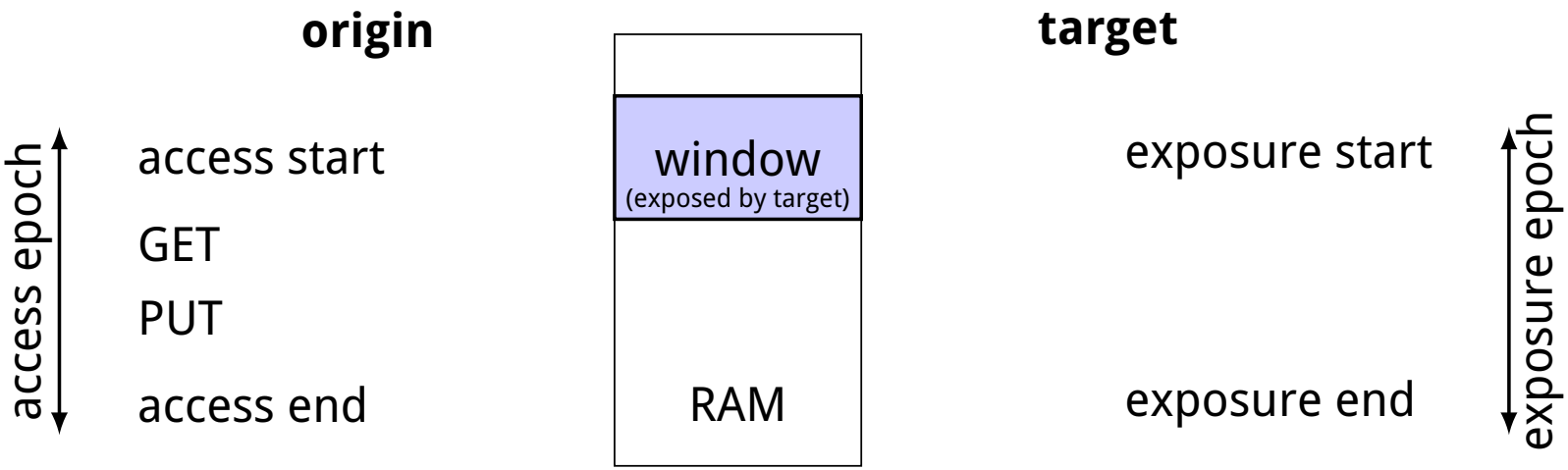

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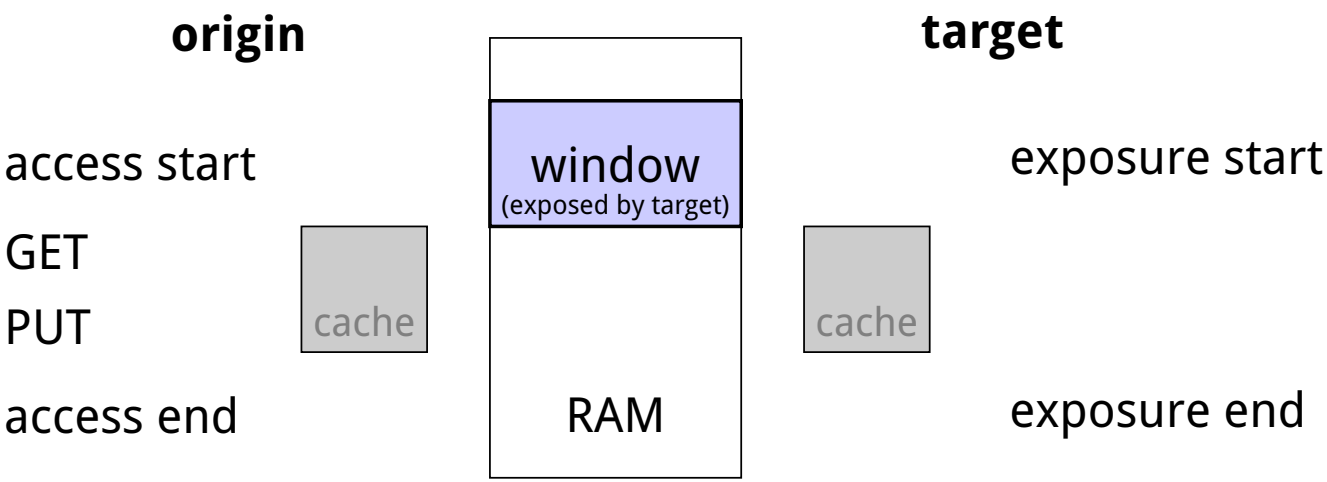

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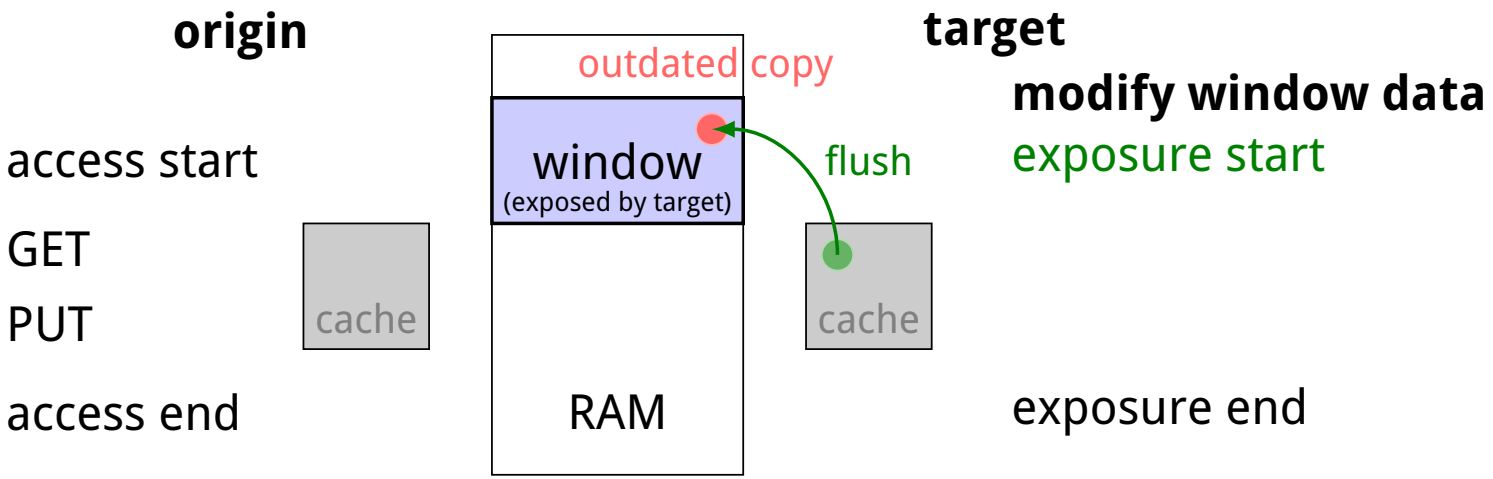

Requirements for Software-Managed Cache Coherence

target/exposure start: write window data back to RAM

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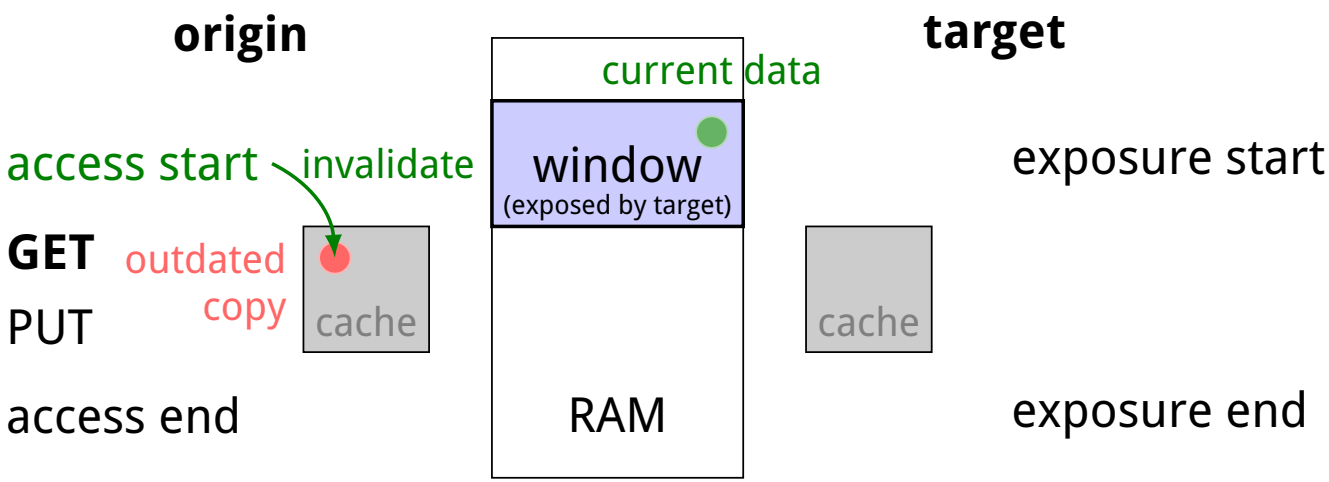

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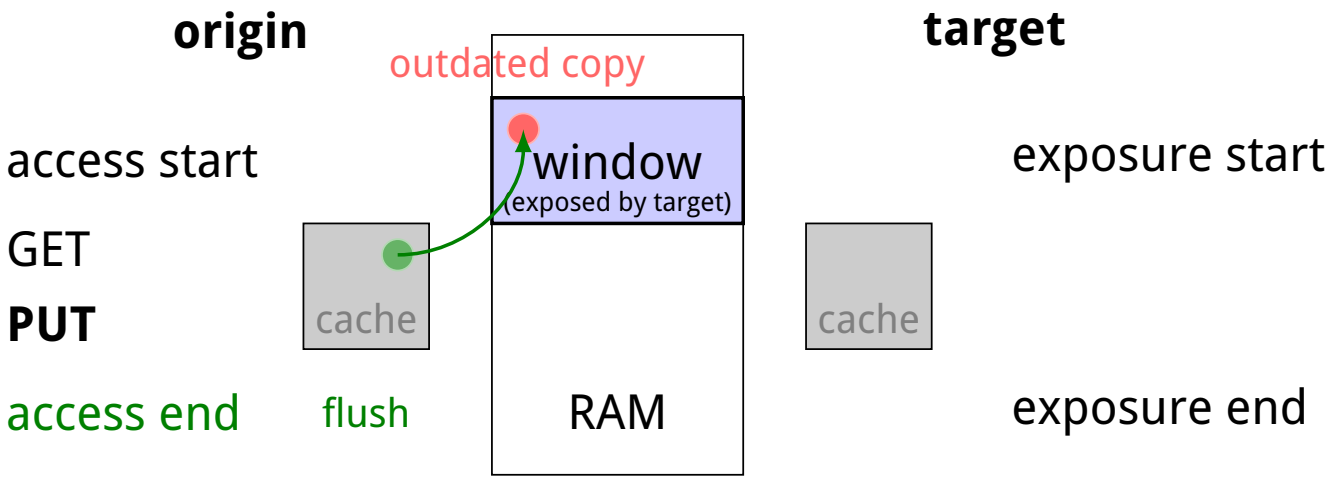

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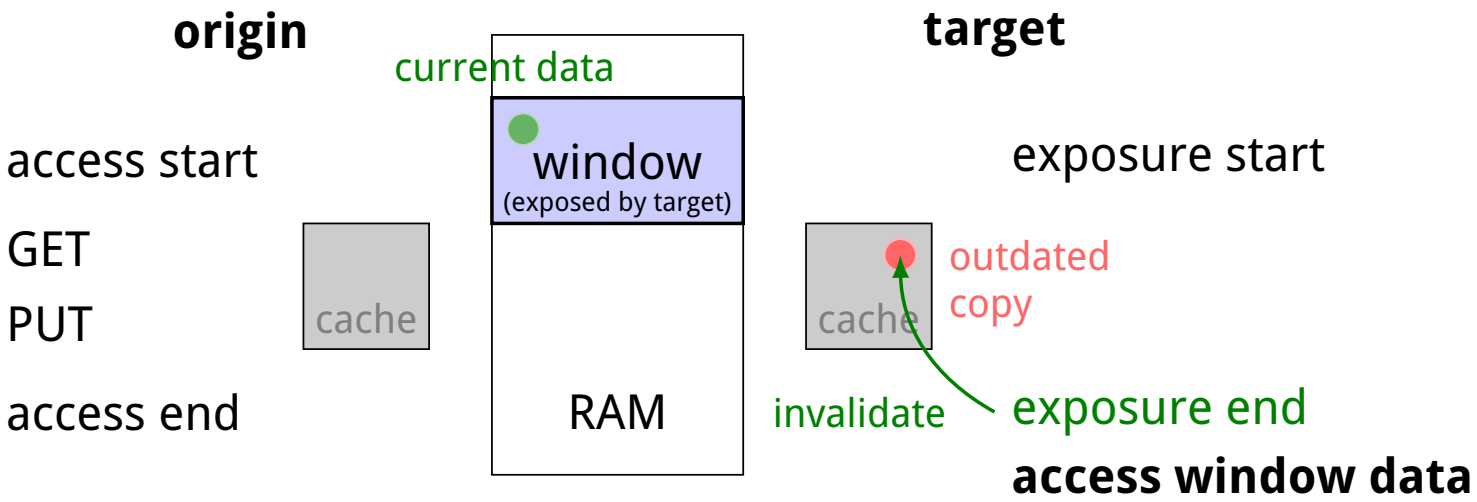

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  $\rightarrow$ issue fast **invalidate instruction**
- but: SCC's write-through has uncached memory performance
  - use write-back configuration as substitute
  - for benchmarks: ensure cache miss on write

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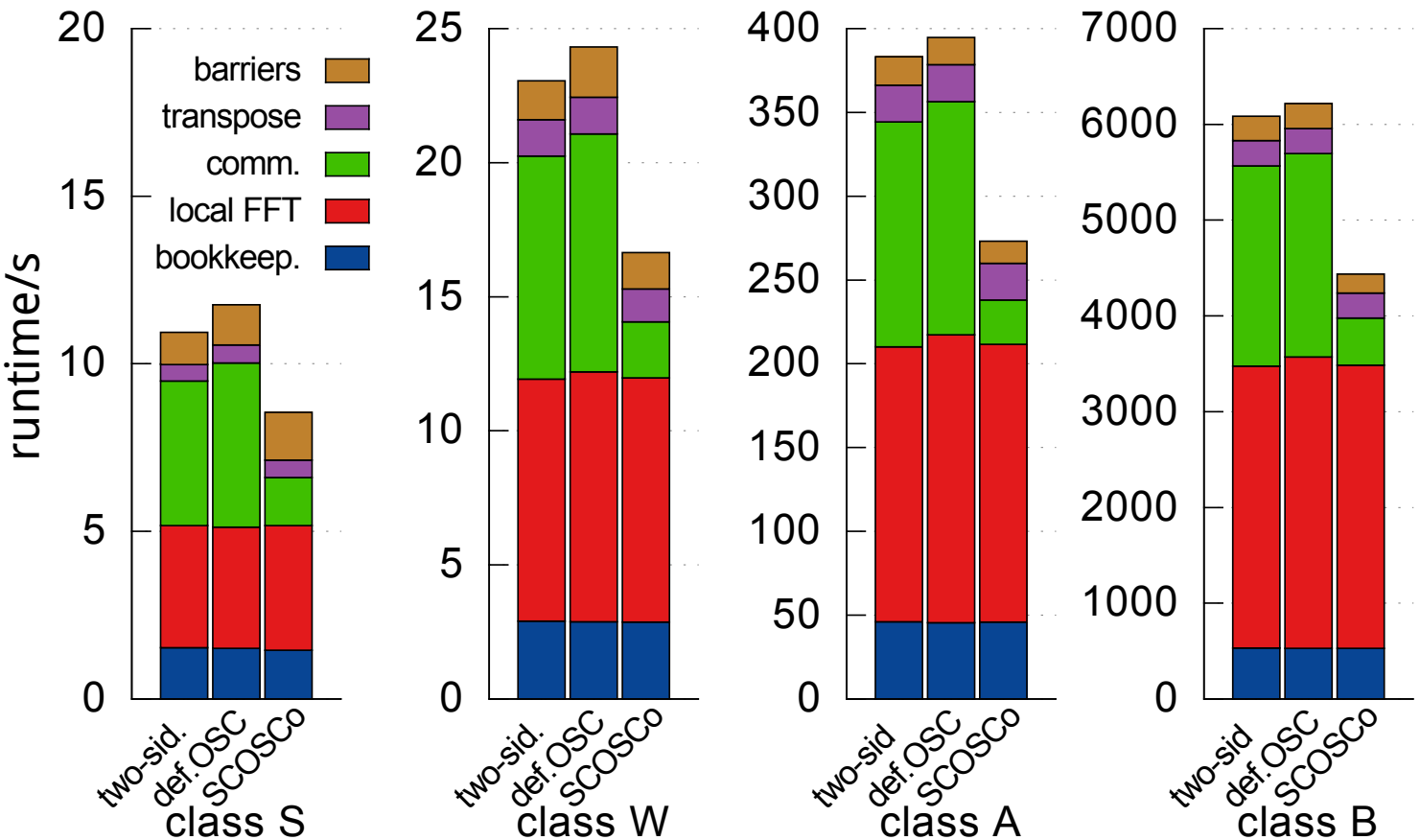

Wishful Thinking for Fast OSC on nCC Systems

Recommendations for Future Systems

potentials for further improvements

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- slow flush to RAM
  - slow performance of working write-through memory (?)
  - (full) cache flush slow anyway

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- slow flush to RAM
- wasteful invalidation
  - removes all window data (not only modified)
  - affects other cached data of same type

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desireable beneficial hardware features in future nCC systems:

- **flushable write-combine buffer** for write-through memory
  - alternative: address range-based flush of modified cache lines

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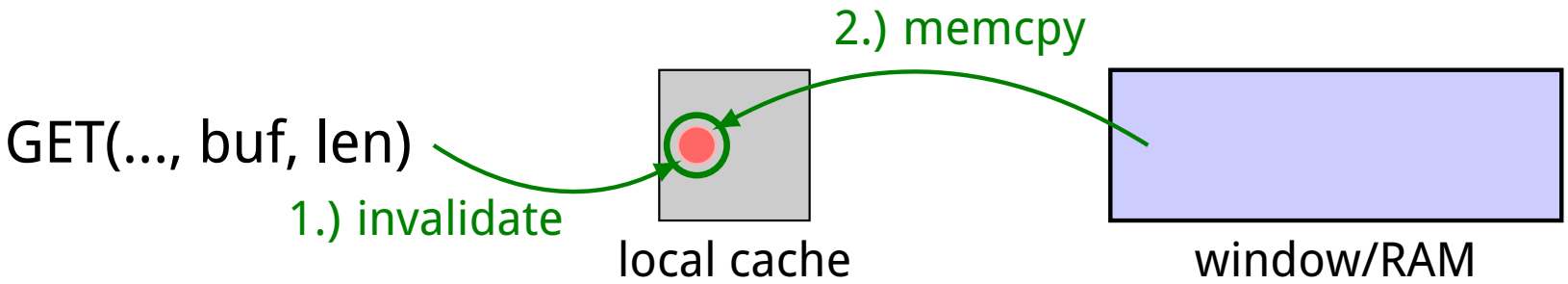

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desireable beneficial hardware features in future nCC systems:

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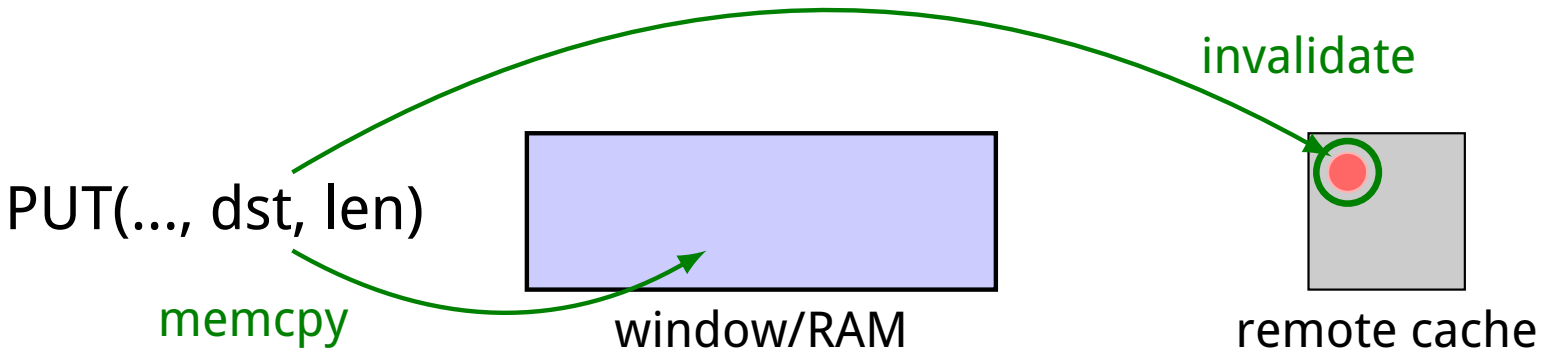
- address **range-based cache invalidation** (for GETs)
- **remote cache invalidation** by address range (for PUTs)



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- address **range-based cache invalidation** (for GETs)
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$\rightarrow$ more explicit control over caches for software

Summary

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- identified beneficial features for future systems
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Thanks for your attention!